CLAIMS

What is claimed is:

1. A method of forming a damascene interconnect barrier layer, the method comprising:

forming a trench in a dielectric layer; and

implanting Ca ions into the sidewalls of the trench; and

forming an inlaid metal conductor in the trench.

2. The method as recited in claim 1 wherein the Ca ion implantation is conducted using a series of tilted implants.

3. The method as recited in claim 2 wherein the series of tilted calcium ion implantations is conducted at a wafer tilt angle ranging from about 0 to 30° and twist angle increments of 90° per rotation.

4. The method as recited in claim 1 wherein the calcium ion implantation generates a calcium concentration profile extending from the surface of the trench sidewall to a depth up to 500 Angstroms.

5. The method as recited in claim 1 wherein the calcium ion implantation generates a peak calcium concentration to a depth in the range from about 50 to 500 Angstroms from the surface of the trench sidewall.

6. The method as recited in claim 1 wherein the series of tilted calcium ion implants is conducted such that about 25% of calcium is implanted in said trench sidewalls for a given twist angle.

7. The method as recited in claim 1 wherein the series of tilted calcium ion implantation steps are conducted at about a 90° angle to the surface of the substrate

8. The method as recited in claim 1 further comprising implanting a concentration of calcium ions into the bottom of the channel using a straight implant.

9. The method as recited in claim 1 further comprising forming a second calcium ion implanted layer above the top surface of the inlaid metal conductor wherein said second calcium ion implantation is conducted with Ca ions using 10 to 80keV energy.

10. The method as recited in claim 9 wherein said second calcium ion implantation is conducted with Ca ions using from 10 to 20keV of the ion energy (or acceleration energy) and a 0 to 30° tilt.

11. The method as recited in claim 9 wherein said second calcium ion implantation is conducted with a 1x $10^{14}cm^{-2}$ to 1x $10^{16}cm^{-2}$ of ion dose.

12. The method as recited in claim 9 wherein said second calcium ion implantation is formed in a low-k layer disposed directly on the top surface of the inlaid conductor.

13. The method as recited in claim 12 wherein the low-k layer has a thickness in the range from about 10 to 500 Angstroms.

14. The method as recited in claim 9 wherein the inlaid conductor is copper and said second calcium ion implantation is formed directly on the top surface of the inlaid conductor.

15. The method as recited in claim 1 wherein the trench is formed in a single damascene process.

16. The method as recited in claim 1 wherein the trench is formed in a dual damascene process.

17. A semiconductor integrated circuit comprising:

a dielectric layer;

an inlaid copper conductor formed in a channel in the dielectric layer; and

a first calcium implant region comprising a concentration of Ca atoms incorporated into the sidewalls of the channel using ion implantation.

18. The integrated circuit as recited in claim 17, wherein the concentration of Ca atoms is positioned within about 500 Angstroms of the surface of the sidewall of the channel.

19. The integrated circuit as recited in claim 18 further comprising a second calcium ion implanted region formed in a low-k layer disposed directly on the top surface of the inlaid conductor.

20. The integrated circuit as recited in claim 17 further comprising a concentration of calcium ions implanted into the bottom of the channel.